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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/593,335

09/19/2006

Simon Deleonibus

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OLIFF & BERRIDGE, PLC

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EXAMINER

QUINN, REGINALD

ART UNIT

PAPER NUMBER

2892

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/593,335	<b>Applicant(s)</b> DELEONIBUS, SIMON	
	<b>Examiner</b> REGINALD QUINN	<b>Art Unit</b> 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 September 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 September 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>9-19-2006</u> .   | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 & 4 rejected under 35 U.S.C. 102(b) as being anticipated by Nishimura et al. (US 5523588 A).

In regards to claim 1:

Nishimura discloses a method for making a field effect transistor comprising a source and a drain connected by a channel controlled by a gate electrode separated from the channel by a gate insulator, the channel, being formed by a diamond-like carbon layer, method successively comprising: deposition of a diamond-like carbon layer (fig. 5B, 53) on a substrate (fig. 5B, 51), deposition of an insulating gate layer (fig. 5B, 54) on the diamond-like carbon layer deposition, on the insulating gate layer, of at least one conducting layer (fig. 5B, 58) and etching (as shown in figures 5B-5C) of the latter so as to form the gate electrode (fig. 5C, 58), deposition of an insulating material (fig. 5D, 582) on flanks (shown in figures 5C-5D) of the gate electrode to form a lateral insulator (fig. 5D, 582), etching (illustrated in figures 5D-6A) of the gate insulating layer, etching (shown in figures 6A-6B ) of the diamond-like carbon layer so as to delineate (as shown in fig. 6B, the resultant etch outlines a channel region) the channel region,

deposition (shown in figures 6A-6B) on each side of the channel, of a semi-conducting material (fig. 6B, 542) designed to form the source (col. 6, lines 12-14) and of a semi-conducting material designed to form the drain (col. 5, lines 12-14).

In regards to claim 4:

The method steps of claim 1 are inherent in the device structure of claim 4.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Ishikura et al (US 6025211) and Nasser-Faili et al. (US 6013191).

1. Nishimura discloses the method as claimed in claim 1.
2. Although Nishimura teaches etching the diamond-like carbon layer, it lacks doing so with isotropic etching.
3. Ishikura teaches isotropic etching (shown in figures 8C-8D) a gold layer (figures 8C-8D, 30) with isotropic etching (col. 7, line 63) forming a cavity (fig. 8D, 75).
4. It would have been obvious to one having ordinary skill in the art at the time of the invention to use the isotropic method of Ishikura in the method of Nishimura for the purpose of forming a retraction under the gate insulating layer to allow as

shown in Ishikura (fig. 8d) one of ordinary skill in the art flexibility in forming a other semiconductor materials in the cavity or retraction under the gate insulating layer (when used in combination with Nishimura) for various purposes.

5. Although, Nishimura and Ishikura teach isotropic etching to form a retraction under the gate insulating layer, they lack isotropic etching of diamond like carbon layer.

6. Nasser-Faili teaches isotropic etching (col. 6, line 1) of diamond (col. 6, line 1).

7. It would have been obvious to one having ordinary skill in the art at the time of the invention to use the isotropic method of Nasser-Faili to etch the diamond layer in Nishimura and Ishikura because doing so is a common method of etching diamond as disclosed in (col. 2 lines 13-19 & col. 1, lines 26-27) Nasser-Faili.

5. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura, Ishikura, and Nasser-Faili as applied to claim 2 above, and further in view of Clevenger et al. (US 6573565 B2).

1. Nishimura, Ishikura, and Nasser-Faili teach the method as claimed in claim 2.

2. Although Nishimura, Ishikura, and Nasser-Faili teach etching of semi-conducting materials in the zones of the substrate not covered by the gate electrode and the lateral insulator (as shown in fig. 6a-6b in Nishimura).

Nishimura, Ishikura, and Nasser-Faili lack doing so using anisotropic etching.

3. Clevenger teaches anisotropic etching of semiconductor materials (col. 7, lines 5-6)
4. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the anisotropic method of Clevenger in the methods of Nishimura, Ishikura, and Nasser-Faili. The anisotropic method of Clevenger (col. 7, lines 5-6) etches diamond. One of ordinary skill in the art would use that anisotropic method in Clevenger to etch undesirable remaining layers of diamond in the device of Nishimura, Ishikura, and Nasser-Faili as well as the other semi-conducting materials, particularly, the dielectric being etched in Nishimura fig. 6a-6b.
6. Claims 5-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Dennard et al. (US 4090289 A).

In regard to claims 5-8,

1. Nishimura discloses a transistor according to claim 4.
2. Nishimura fails to disclose a transistor according to claim 4, wherein the channel comprises n-type dopants so as to form a PMOS type transistor and/or p-type dopants to form a NMOS type transistor, having substantially the same dimensions.
3. Dennard discloses a channel comprising p type dopants (inherent in a nmos transistor) forming a nmos transistor (col. 5, lines 52-63), a channel comprising n type dopants (inherent in a pmos transistor) to form pmos transistors (col. 5, lines

52-63), at least one pmos and nmos transistor having substantially the same dimensions (as illustrated in fig. 6).

4. Dennard does not disclose CMOS (complimentary MOS comprises PMOS and NMOS). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form PMOS and NMOS transistors using the device of Dennard in the method of Nishimura because such CMOS structures are typical and conventional in the art.

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 2006/0151844 A1 anticipates claim 1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to REGINALD QUINN whose telephone number is (571)270-5017. The examiner can normally be reached on Mon.-Fri. 7:30am-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Reginald Quinn/

/Thao X Le/  
Supervisory Patent Examiner, Art  
Unit 2892